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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
QUINTO, KEVIN V

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/044,493	Applicant(s) YU ET AL	
	Examiner Kevin Quinto	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *11-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-10, drawn to a semiconductor device, classified in class 257, subclass 377.

II. Claims 11-19, drawn to method of making a semiconductor device, classified in class 438, subclass 199.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the gate dielectric can be selectively formed instead of requiring removal in an area laterally surrounding the gate electrode.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with David Galin on June 19, 2002, a provisional election was made with traverse to prosecute the invention of the semiconductor device, claims 1-10. Affirmation of this election must be made by applicant in replying to this Office action.

Claims 11-19 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Gardner et al. (USPN 6,002,150).

7. In reference to claims 1 and 2, Gardner et al. (USPN 6,002,150, hereinafter referred to as the "Gardner" reference) discloses a similar device. Figure 9 of Gardner illustrates a MOSFET with a semiconductor body (not labeled) disposed between a source and a drain (126). The source and drain (126) have a silicide formed on their upper surfaces. There is a gate electrode (112) disposed over the body which defines a channel interposed between the source and the drain (126). There is a gate dielectric (110) made from a high-K (dielectric constant) material. The high dielectric constant material is described with regard to figure 2 in Gardner (column 6, lines 45-52). This gate dielectric (110) separates the gate electrode (112) and the body.

8. In reference to claims 3 and 4, Gardner discloses the use of a metal containing material in the gate electrode (112). Metal containing materials such as tungsten and tungsten nitride are disclosed by Gardner as possible materials for the gate electrode (column 7, lines 28-31).

9. In reference to claim 5, Gardner discloses the use of barium strontium titanate as the gate dielectric (column 6, lines 45-52).

10. In reference to claim 6, Gardner uses a buffer layer (102, figure 2) which is between the body and the gate dielectric (110).

11. Claims 1-6 and 8-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Oowaki et al. (USPN 6,278,165 B1).

12. In reference to claims 1 and 2, Oowaki et al. (USPN 6,278,165 B1, hereinafter referred to as the "Oowaki" reference) discloses a similar device. Figure 2 of Oowaki illustrates a MOSFET with a semiconductor body (1) disposed between a source and a drain (2). Oowaki discloses that the source and drain can be silicided (column 6, lines 12-15). There is a gate electrode (6) disposed over the body which defines a channel interposed between the source and the drain (2). There is a gate dielectric (5) made from a high-K (dielectric constant) material (column 6, lines 54-56). This gate dielectric (5) separates the gate electrode (6) and the body (1).

13. In reference to claims 3 and 4, Oowaki discloses the use of a metal containing material in the gate electrode (6). Metal containing materials such as titanium nitride, tantalum nitride, tantalum, titanium, palladium, platinum are disclosed by Oowaki as possible materials for the gate electrode (column 17, lines 1-6).

14. In reference to claim 5, Oowaki claims the use of high dielectric constant materials titanium oxide and aluminum oxide as the gate dielectric (claim 6).

15. In reference to claim 6, Oowaki uses a buffer layer (3) which is between the body (1) and the gate dielectric (5).

16. So far as understood in claim 8, Oowaki discloses that the silicide can be formed with nickel (column 6, lines 12-15). It is understood that the layer of semiconductor material, which is a part of the nickel silicide, is a part of the body (1).

17. In reference to claim 9, Oowaki discloses the use of a liner (3) which is disposed adjacent sidewalls defined by the gate electrode (6) and the gate dielectric (5).

18. In reference to claim 10, Oowaki discloses (column 16, lines 56-60) that the device can be formed on an SOI substrate (a semiconductor film disposed on an insulating layer, the layer being disposed on a semiconductor substrate).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oowaki et al. (USPN 6,278,165 B1) in view of Raajimakers et al. (United States Patent Application Publication No. US 2001/0031562 A1).

21. In reference to claim 7, Oowaki does not disclose the use of an oxide buffer layer. However it is well known in the art to provide an oxide buffer layer between a substrate and a high dielectric constant insulating film. Raajimakers et al. (United States Patent Application

Publication No. US 2001/0031562 A1, hereinafter referred to as the "Raajimakers" reference) discloses that a thin silicon oxide layer improves the interface between silicon and a high dielectric constant film (p.1, paragraph 7 and p.3, paragraph 33). It would therefore be obvious to use an oxide buffer layer in the device of Oowaki so as to attain this benefit. Oowaki and Raajimakers teach all of the claimed invention except for the exact thickness of the oxide layer. Although Oowaki and Raajimakers do not teach the exact oxide thickness as that claimed by Applicant:

> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

Therefore claim 7 is not patentably distinguishable over the Oowaki and Raajimakers references.

22. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (USPN 6,002,150) in view of Raajimakers et al. (United States Patent Application Publication No. US 2001/0031562 A1).

23. In reference to claim 7, Gardner does not disclose the use of an oxide buffer layer. However it is well known in the art to provide an oxide buffer layer between a substrate and a high dielectric constant insulating film. Raajimakers discloses that a thin silicon oxide layer improves the interface between silicon and a high dielectric constant film (p.1, paragraph 7 and p.3, paragraph 33). It would therefore be obvious to use an oxide buffer layer in the device of Gardner so as to attain this benefit. Gardner and Raajimakers teach all of the claimed invention except for the exact thickness of the oxide layer. Although Gardner and Raajimakers do not teach the exact oxide thickness as that claimed by Applicant:

> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

Therefore claim 7 is not patentably distinguishable over the Gardner and Raajimakers references.

24. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (USPN 6,002,150) in view of Xiang et al. (USPN 5,937,315).

25. In reference to claim 8, Gardner discloses the use of a metal silicide (column 8, lines 23-44) on the source and drain (126). It is understood that the layer of semiconductor material, which is a part of the metal silicide, is a part of the body. Gardner does not disclose the use of nickel silicide (Gardner uses titanium silicide and cobalt silicide). However the use of nickel silicide is well known in the art. Xiang et al. (USPN 5,937,315, hereinafter referred to as the "Xiang" reference) discloses that nickel silicide provides the advantages of low sheet resistance and low contact resistance (column 4, lines 34-38). It would therefore be obvious to construct the device of Gardner with a nickel silicide in order to attain these benefits.

26. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (USPN 6,002,150) in view of Venkatesan et al. (USPN 5,736,435).

27. In reference to claim 10, Gardner does not disclose the use of an SOI substrate (a semiconductor film disposed on an insulating layer, the layer being disposed on a semiconductor substrate). However the use of an SOI substrate is well known in the art. Venkatesan et al. (USPN 5,736,435, hereinafter referred to as the "Venkatesan" reference) discloses that SOI provides the advantages of reduced junction capacitance, large drive currents, high transconductance values, and immunity to short channel effects (column 1, lines 35-55). It would therefore be obvious to construct the device of Gardner on an SOI substrate so as to attain these benefits.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ
June 27, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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